In the Claims:

Please amend claims 48-50 as shown below:

48.(Currently Amended) The method of claim 29, ~~wherein the~~ wherein the memory storage unit is a molecular transistor memory storage unit.

49.(Currently Amended) The method of claim 29, ~~wherein the~~ wherein the memory storage unit is a single electron transistor memory storage unit.

50.(Currently Amended) The method of claim 29, ~~wherein the~~ wherein the memory storage unit is a nano-transistor memory storage unit.

Please amend claims 67-69 as shown below:

67.(Currently Amended) The method of claim 53, ~~wherein the~~ wherein the memory storage unit is a molecular transistor memory storage unit.

68.(Currently Amended) The method of claim 53, ~~wherein the~~ wherein the memory storage unit is a single electron transistor memory storage unit.

69.(Currently Amended) The method of claim 53, ~~wherein the~~ wherein the memory storage unit is a nano-transistor memory storage unit.

REMARKS

The present Amendment is being made to correct formal matters in several claims that do not change their scope. Specifically, in several dependent claims, a further limitation introduced by the phrase "wherein the" had this phrase repeated. Consequently, the "wherein the wherein the ..." has now been replaced with "wherein the ...".

The present amendment is needed to remove this redundant language. As it does not change the substance of the claims, it is believed the changes require no additional examination and do not affect the patentability of the claims. These changes were not presented earlier as they have only recently been noted during a review of the allowed claims.

Applicants respectfully request that this Amendment be entered.

Respectfully submitted,

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APPENDIX

1. A method of reading the data content of a non-volatile memory storage unit, comprising:

applying a set of sense voltage waveforms to the terminals of the memory storage unit during a read interval;

measuring a parameter value related to the data content of the memory storage unit during the read interval, wherein the measured value for the parameter includes the contribution of a noise component;

applying an episodic stimulus to the memory storage unit during the read interval, wherein the level of stimulus affects the parameter value and whereby the contribution of the noise component is reduced.

2. The method of claim 1, wherein the parameter is a current.

3. The method of claim 1, wherein the parameter is a voltage.

4. The method of claim 1, wherein the parameter is a time.

5. The method of claim 1, wherein the parameter is a frequency.

6. The method of claim 1, wherein the memory storage unit is a floating gate transistor and the measuring a parameter value comprises applying a non-periodic voltage to a first control gate of the transistor, and wherein the parameter is measured between a first and a second source/drain region of the transistor.

7. The method of claim 6, wherein the episodic stimulus is a periodic voltage waveform.

8. The method of claim 7, wherein the floating gate transistor further includes a select gate and the episodic stimulus is applied to the select gate.

9. The method of claim 7, wherein the episodic stimulus is applied to the first control gate of the transistor.

10. The method of claim 7, wherein the episodic stimulus is applied to the substrate of the transistor.

11. The method of claim 10, wherein the floating gate transistor has dual floating gates, the first control gate being located over a first of the dual floating gates, and further comprises a second control gate over the second of the dual floating gates, wherein the select gate is situated between the two control gates.

12. The method of claim 7, wherein the periodic voltage has a sinusoidal wave form.

13. The method of claim 7, wherein the periodic voltage has a rectangular wave form.

14. The method of claim 7, wherein the periodic voltage has a trapezoidal wave form.

15. The method of claim 6, wherein the parameter is the current flowing in a channel region of the floating gate transistor.

16. The method of claim 6, wherein the parameter is a voltage required to established a predetermined current.

17. The method of claim 6, wherein the episodic stimulus is a single voltage pulse.

18. The method of claim 6, wherein the read interval comprises a first phase and a subsequent second phase, wherein the measuring a parameter is performed during

the second phase and the applying a set of sense voltage waveforms begins during the first phase.

19. The method of claim 18, wherein the episodic stimulus are multiple voltage pulses.

20. The method of claim 18, wherein the episodic stimulus is applied during the second phase.

21. The method of claim 18, wherein the episodic stimulus is applied during the first phase.

22. The method of claim 1, wherein the memory storage unit is a magnetic memory cell and the episodic stimulus is a magnetic field.

23. The method of claim 1, wherein the wherein the memory storage unit is a molecular transistor memory storage unit.

24. The method of claim 1, wherein the wherein the memory storage unit is a single electron transistor memory storage unit.

25. The method of claim 1, wherein the wherein the memory storage unit is a nano-transistor memory storage unit.

26. The method of claim 1, wherein said applying an episodic stimulus is invoked in response to an error control coding result.

27. The method of claim 1, wherein said read interval comprises a first portion and a subsequent second portion, and wherein said applying a set of sense voltage waveforms comprises:

applying a first set of sense voltage waveforms to the terminals of the memory storage unit during the first portion of the read interval; and

applying a second set of sense voltage waveforms to the terminals of the memory storage unit during the second portion of the read interval;

wherein said measuring the parameter value comprises:

measuring the parameter value related to the data content of the memory storage unit during the first portion of the read interval; and

measuring a parameter value related to the data content of the memory storage unit during the second portion of the read interval; and

wherein said applying an episodic stimulus is performed during the second portion of the read interval in response to said measuring the parameter value related to the data content of the memory storage unit during the first portion of the read interval.

28. The method of claim 27, wherein said applying an episodic stimulus is invoked in response to an error control coding result.

29. A method of operating of a non-volatile memory, comprising:

applying a set of voltages to a storage unit of the non-volatile memory during an interval;

determining the conduction characteristics of the storage unit in response to the set of voltages, wherein the set of voltages includes an episodic stimulus component.

30. The method of claim 29, wherein the determining the conduction characteristics comprises measuring a current.

31. The method of claim 29, wherein the determining the conduction characteristics comprises measuring a voltage.

32. The method of claim 29, wherein the determining the conduction characteristics comprises measuring a time.

33. The method of claim 29, wherein the determining the conduction characteristics comprises measuring a frequency.

34. The method of claim 29, wherein the memory storage unit is a floating gate transistor and the set of voltages further includes applying a non-periodic voltage to a first control gate of the transistor, wherein the determining the conduction characteristics includes measuring a parameter between a first and a second source/drain region of the transistor during a read interval.

35. The method of claim 34, wherein the episodic stimulus is applied to the control gate of the transistor.

36. The method of claim 34, wherein the episodic stimulus is applied to the substrate of the transistor.

37. The method of claim 34, wherein the floating gate transistor further comprises a select gate and the episodic stimulus is applied to the select gate.

38. The method of claim 37, wherein the floating gate transistor has dual floating gates, the first control gate being located over the first of the dual floating gates, and further comprises a second control gate over the second of the dual floating gates, wherein the select gate is situated between the two control gates.

39. The method of claim 34, wherein the parameter is the current flowing in a channel region of the floating gate transistor.

40. The method of claim 34, wherein the parameter is a voltage required to established a predetermined current.

41. The method of claim 34, wherein the read interval comprises a first phase and a subsequent second phase, wherein the measuring a parameter is performed during the second phase and applying a set of sense voltage waveforms beginning during the first phase.

42. The method of claim 41, wherein the episodic stimulus is applied the second phase.

43. The method of claim 41, wherein the episodic stimulus is applied the first phase.

44. The method of claim 29, wherein the episodic stimulus is a voltage having a sinusoidal waveform.

45. The method of claim 29, wherein the episodic stimulus is a voltage having a rectangular wave form.

46. The method of claim 29, wherein the episodic stimulus is a voltage having a trapezoidal wave form.

47. The method of claim 29, wherein the memory storage unit is a magnetic memory cell and the episodic stimulus is a magnetic field.

48.(Currently Amended) The method of claim 29, wherein the memory storage unit is a molecular transistor memory storage unit.

49.(Currently Amended) The method of claim 29, wherein the memory storage unit is a single electron transistor memory storage unit.

50.(Currently Amended) The method of claim 29, wherein the memory storage unit is a nano-transistor memory storage unit.

51. The method of claim 29, wherein said determining the conduction characteristics of the storage unit comprises:

determining a first time the conduction characteristics of the storage unit in response to the set of voltages; and

subsequently determining a second time the conduction characteristics of the storage unit in response to the set of voltages, wherein the episodic stimulus component is applied only during said determining a second time.

52.(Previously Amended) The method of claim 51, wherein said subsequently determining a second time the conduction characteristics of the storage unit is in response to error control coding result.

53.(Previously Amended) A non-volatile memory, comprising:

a memory storage unit;

a sense amplifier connected to the memory storage unit for determining the state of the memory storage unit in response to a set of read voltages; and

drivers connected to the memory storage unit for applying the set of read voltages to the memory storage unit, the set of read voltages comprising:

a sense voltage condition; and

an episodic stimulus voltage condition.

54. The memory of claim 53, wherein the sense amplifier operates by sensing a current.

55. The memory of claim 53, wherein the sense amplifier operates by sensing a voltage.

56. The memory of claim 53, wherein the memory storage unit is a floating gate transistor and the sense voltage condition includes applying a voltage to a first control gate of the transistor, wherein the sense amplifier measures a parameter between a first and a second source/drain region of the transistor.

57. The memory of claim 56, wherein the episodic stimulus voltage condition is applied to a control gate of the transistor.

58. The memory of claim 56, wherein the episodic stimulus voltage condition is applied to the substrate of the transistor.

59. The memory of claim 56, wherein the floating gate transistor further comprises a select gate and the episodic stimulus voltage condition is applied to the select gate.

60. The memory of claim 59, wherein the floating gate transistor has dual floating gates, the first control gate being located over a first of the dual floating gates, and further comprises a second control gate over the second of the dual floating gates, wherein the select gate is situated between the two control gates.

61. The memory of claim 56, wherein the parameter is the current flowing in a channel region of the floating gate transistor.

62. The memory of claim 56, wherein the parameter is a voltage required to establish a predetermined current.

63. The memory of claim 53, wherein the episodic stimulus voltage condition is a periodic voltage having a rectangular wave form.

64. The memory of claim 53, wherein the episodic stimulus voltage condition is a periodic voltage having a trapezoidal wave form.

65. The memory of claim 53, further comprising:

an error control code section coupled to the sense amplifier and to the drivers, wherein said drivers apply the episodic stimulus voltage condition in response to a control signal from the error control code section.

66. The method of claim 53, wherein the memory storage unit is a magnetic memory cell and the episodic stimulus is a magnetic field.

67.(Currently Amended) The method of claim 53, wherein the memory storage unit is a molecular transistor memory storage unit.

68.(Currently Amended) The method of claim 53, wherein the memory storage unit is a single electron transistor memory storage unit.

69.(Currently Amended) The method of claim 53, wherein the memory storage unit is a nano-transistor memory storage unit.

70. The memory of claim 53, wherein the non-volatile memory comprises an array of storage units of which said memory storage unit is a member, further comprising:

a booster line connected between one of said drivers and a portion of the array including said memory storage unit whereby said episodic stimulus voltage condition is applied.